Wide Dynamic Range Low Light Level CMOS Image Sensor

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Abstract—**This paper describes a CMOS image sensor technology suitable for the next generation of scientific cameras. We describe a prototype sensor with 320x240 pixels based on this technology. The sensor features 8 different types of 5T pixels with pinned photodiodes. All of the pixels have a 6.5um pitch and include an integrated micro-lens. The measured peak quantum efficiency of the sensor is greater than 50% at 550nm, and the read noise is less than 1e- RMS at room temperature. The linear full well capacity is greater than 40ke-, the dark current is less than 3.8pA/cm^2 at 20°C, and the MTF at 77 lp/mm is 0.4 at 600nm. The sensor also achieves an intra-scene linear dynamic range of greater than 92dB (40000:1) at room temperature.**

Index Terms—Wide dynamic range, low noise, CMOS image sensor

I. Introduction

As bio-technology transitions from research and development to high volume production, dramatic improvements in image sensor performance will be required to support the throughput and cost requirements of this market. This includes higher resolution, higher frame rates, higher quantum efficiencies, increased system integration, lower read-noise, and lower device costs [1]. Although CCDs and electron multiplying CCDs dominate this market today they are mature technologies that offer little promise of meeting the future needs of this market.

In this paper we present a CMOS image sensor technology suitable for the next generation of scientific cameras. We describe a prototype sensor with 320x240 pixels based on this technology. The sensor features 8 different types of 5T pixels with pinned photodiodes. All of the pixel have a 6.5um pitch and include an integrated micro-lens. The measured peak quantum efficiency of the sensor is greater than 50% at 550nm, and the read noise is less than 1e- RMS at room temperature. The linear full well capacity is greater than 40ke-, the dark current is less than 3.8pA/cm^2 at 20°C, and the MTF at 77 lp/mm is 0.4 at 600nm. The sensor also achieves an intra-scene linear dynamic range of greater than 92dB (40000:1) at room temperature.

The prototype chip has on-chip dual column level amplifiers and 11-bit single slope analog to digital converters (ADC) for high speed readout and wide optical dynamic range. The dual column level amplifier/ADC pairs have independent gain settings, and the final image is reconstructed by combining pixel readings from both the high and low gain readout channels to achieve a wide intra-scene dynamic range. The bandwidths of the column level amplifiers and ADCs are programmable to optimize the sensor read noise for the selected sensor frame rate. The sensor can operate up to a line rate of 111 kHz or a frame rate of 462 Hz. The high speed digital readout electronics allow pixels to be scanned out at up to 287 MHz.

The remainder of the paper is organized as follows: in Section II the sensor operation, architecture, and circuitry are described, in Section III the measurement methods and results are presented, and finally in Section IV we conclude the paper.

II. Sensor Operation

Figure 1 shows the image sensor block diagram. The image sensor consists of an array of 320x240 6.5µm pixels, row and column shift registers, 320 high gain and low gain column level amplifiers and 640 11-bit single slope ADCs, a high speed 22-bit digital readout multiplexer, bias generators, and a bandgap based proportional to absolute temperature (PTAT) sensor. The image sensor operates at pixel rates up to 287 MHz and uses standard 1.8V HSTL I/Os for clock and data signals.

The sensor array consists of eight different pixel types, arranged in 8 columns of 40x240 pixels. Each pixel type has different photodiode and transfer gate sizes. These pixel variations were designed to determine the optimal pixel for low light level applications. Micro-lenses are used on all of the pixels. Some of the sensors also have Bayer pattern RGB color filter arrays [2]. Figure 2 shows a simplified schematic of the 5T pinned photodiode pixel. The charge transfer transistor connected to “TX1” is used to move charge from the pinned photodiode to the floating diffusion node. The source follower transistor size was optimized to minimize read out noise [3]. The reset transistor forces the floating diffusion node to “Vrst” when “reset” is high. When “word” is high the source follower is connected to the bit line and the voltage on the floating diffusion is readout. The transistor connected to TX2 functions as a voltage controlled anti-blooming drain and a global reset device [4].

The row shift register is located at the left side of the chip. The row shift register selects one row of pixels at a time by enabling the "word" line in a given row. During that time, the floating diffusion node in the selected pixel is reset, the reset voltage is read out then the transfer gate is turned on, via TX1, and the integrated charge on the pinned photo-diode is transferred to the floating diffusion node. The signal voltage on the floating diffusion node is read out again. The reset and signal voltages are initially stored on sampling capacitors of both column level amplifiers (high gain and low gain); then the analog data is transferred to a double buffered analog memory (capacitor bank). Then the analog data (stored in the capacitor bank) is digitized using dual 11-bit single slope ADCs. Using the column shift register the double buffered digital data is read out of the sensor. Afterward, the next row is selected and the read out processes continues in a similar fashion. The photodiode inside each pixel starts integration once the transfer gate is turned off. In this scheme, each row of pixels will have the same length of integration time, but a different start and ending time, therefore this scheme is called "rolling shutter".

The sensor has a 22-bit digital output port operating at up to 287 MHz. The digital data at the column is transferred to the output pins using a two level 320:1 digital multiplexer. Note that each pixel is simultaneously readout twice, once through a high gain amplifier and once through a low gain amplifier. Both the high gain amplifier and the low gain amplifier outputs are digitized to 11 bits. The maximum frame rate of the sensor is limited by the settling time of the column amplifiers, i.e. 9us. The maximum frame rate of the sensor is 462 frames per second.

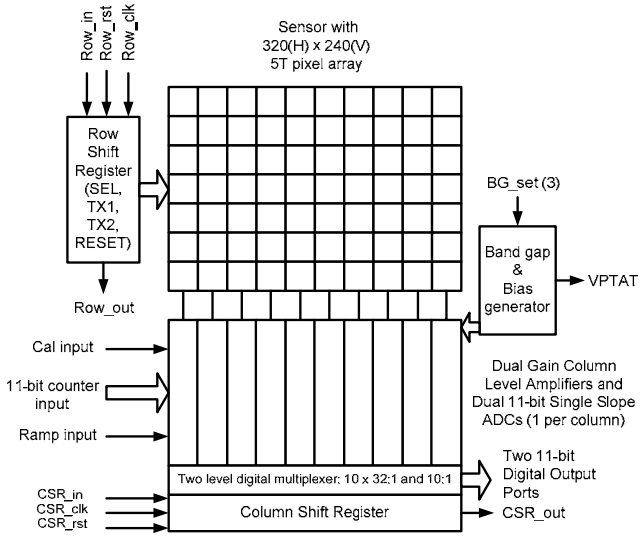

Figure 1. Sensor Block Diagram

Separate power supplies are used for pixel core, analog amplifiers and ADC, pad ring, and digital circuitry. Common ground is used in the entire chip. A power down pin is used to shut down all the bias and analog circuits. Internally, one reference circuit generates a 100uA bias current which in turn generates different bias voltages for column amplifiers and the pixel array.

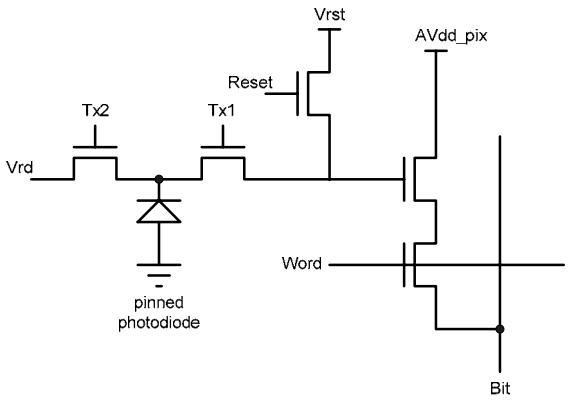

Figure 2. 5T Pixel Schematic

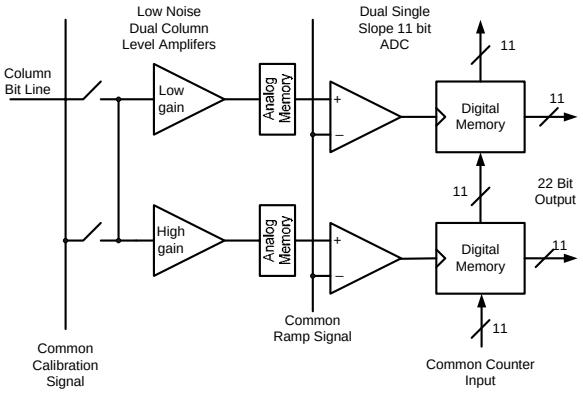

Figure 3. Column level amplifier and ADC block diagram

Figure 3 shows the amplifier and ADC architecture used in each column of the sensor. This architecture was selected to minimize the read noise and maximize the dynamic range simultaneously. There are two amplifiers per column with fixed gains of 30x and 1x respectively. These gain values were selected to minimizing the dip in the sensor SNR when the user switches between the high gain data and the low gain data. Each column also contains two 11-bit single slope ADCs. The amplifier outputs and the ADC outputs are double buffered to maximize the line rate of the sensor. Each column has a reference input that can be multiplexed into the circuit to aid in correcting column level gain and offset fixed pattern noise (FPN). The 22 bit data in each column is transmitted to the output using a 32:10:1 digital multiplexer. The final output data is registered at the output pins to minimize the clock to data skew for high speed operation.

III. RESULTS

Most of the performance parameters were estimated using a pixel level photon transfer based method [5]. These performance metrics include conversion gain, read noise, full well capacity, linearity, pixel response non-uniformity, dark current, dark current non-uniformity and fixed pattern noise. The QE was estimated using the method described in [6], and the MTF was estimated using the ISO12233 standard. Pixel type 7 has the best overall performance, and therefore the figures only display data from these pixels. All of the data was collected using a line time of 64us, and integration time was varied based on the measurement. The sensor temperature was not controlled, but it was measured for each data set. The measured sensor parameters are shown in Table 1. A captured image frame is shown in Figure 4.

The high gain read noise distribution of pixel 7 is shown in Figure 5, and the low gain read noise distribution of pixel 7 is shown in Figure 6. The high gain read noise distribution is dominated by pixel level noise sources. These include source follower white 1/f and RTS noise, and transfer gate / coupling noise. The low gain read noise distribution is dominated by the column level amplifier and ADCs.

Although the n region of the pinned photodiode and the size of the transfer gate were varied significantly from pixel type to pixel type the dark current stayed relatively constant. This implies that the dark current is not an edge or depletion based effect. The dominate leakage component is likely caused by carrier diffusion from the undepleted region of the pixel [7]. The dark current doubling rate is about 7°C at room temperature.

The quantum efficiency (QE) of the sensor, defined as the number of electrons collected divided by the number of incident photons, is shown in Figure 7. The number of incident photons was calculated based on 6.5µm x 6.5µm pixel area.

The modulation transfer function (MTF) of the sensor is shown in Figure 8. The upper function is the vertical MTF and lower function is the horizontal MTF. The pixel has a metal aperture to protect the readout electronics and this causes the MTF to be different in the vertical and the horizontal directions. Note that the MTF was measured with a 0.26 NA diffraction limited microscope lens. The sensor MTF was determined by de-convolving the lens MTF from the measured system MTF.

The sensor SNR as a function of 550nm illumination energy is shown in Figure 9. The dynamic, defined as the low gain full well capacity divided by the high gain read noise, is greater than 92dB (40000:1) and the SNR dip between the high gain channel and the low gain channel is -0.2dB.

TABLE I
SENSOR PROPERTIES (PIXEL 7)

Parameters	High gain channel	Low gain channel
Conversion gain (DN/e-)	2.1	0.065
Read noise (e- RMS)	0.80 (median) 1.15 (mean) 1.10 (std)	7.2 (median) 7.0 (mean) 1.5 (std)
Dark Current (e-/pixel/sec) @ 20C	9	9
Full well capacity (e-)	1.4K	42K
Linearity (% RMS)	1.3	0.15
Dynamic range	1750 (median)	5800 (median)
Max pixel clock (MHz)	287	287
Gain FPN (DN/e-RMS)	0.084	3.9e-5
DSNU (e-/pixel/sec RMS) @ 20C	3.5	3.5
Offset FPN (e- RMS)	13	210

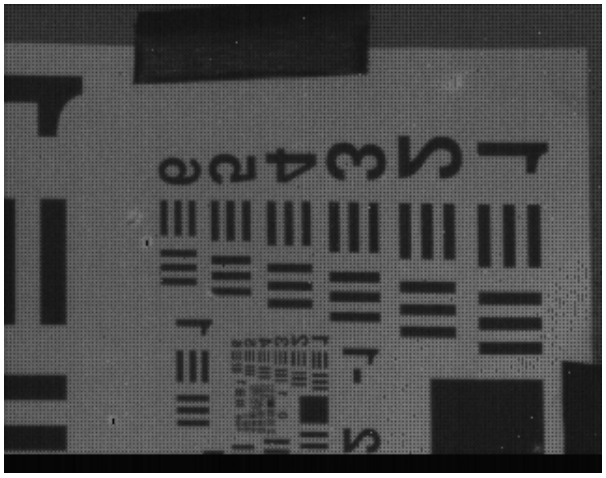

Figure 4. Sample captured image frame with RGB color filter array

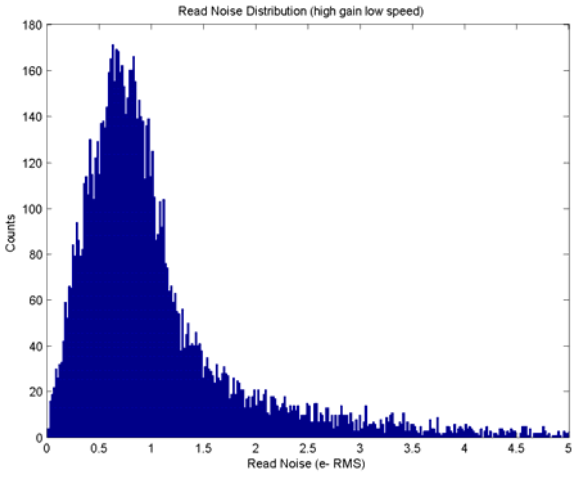

Figure 5. High gain channel read noise distribution of pixel 7

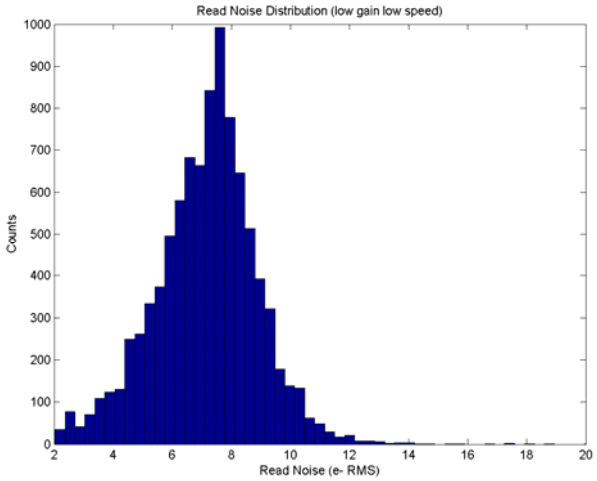

Figure 6. Low gain channel read noise distribution of pixel 7

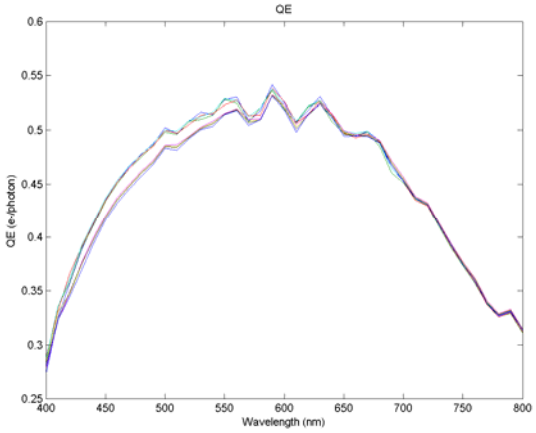

Figure 7. Measured QE of each pixel type

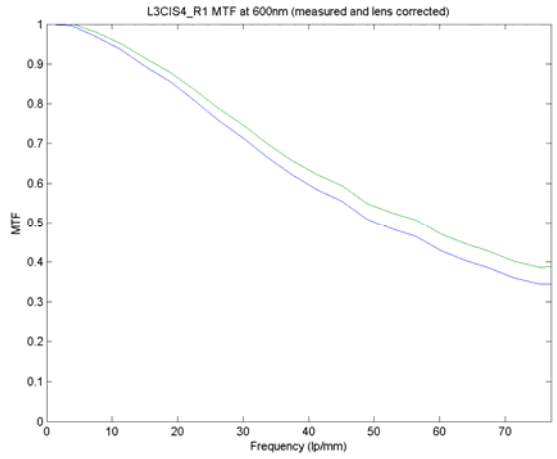

Figure 8. Measured MTF of pixel 7 at 600 nm (green curve is vertical MTF and blue curve is horizontal MTF)

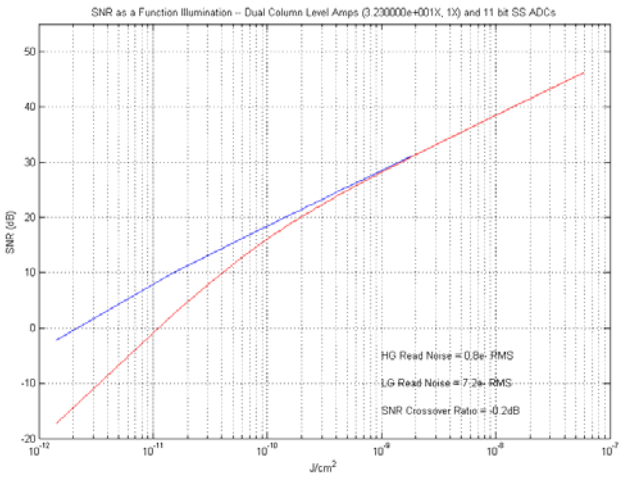

Figure 9. Signal to noise ratio of pixel 7 (high gain channel – blue curve, low gain channel – red curve)

IV. Conclusions

We have presented a 320x240 pixel prototype CMOS image sensor with dual column level amplifiers and 11-bit ADCs. This sensor achieves a median read noise of 0.8e- RMS, a dynamic range greater than 40,000:1, a peak QE greater than 50%, and an MTF at 600nm of approximately 40%.

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